

GOVERNMENT POLYTECHNIC GAJENDRAGAD
Department of Electronics and Communication Engg

Time table (Even Semester)

Year: 2019-20

Semester - 2

Day	9-10	10-11	11-12	12-1	1-2	2-3	3-4	4-5
Mon	← ENGLISH →	→	SCD		LUNCH BREAK	← Math Sim Lab →		
Tue	← ENGLISH →	→	SCD			← Digital Electronics lab-I →		
Wed	← ENGLISH →	→	SCD					
Thu	← Engg.Maths-II →	→	SCD			← SCD Lab →		
Fri	← Engg.Maths-II →	→	SCD					
Sat	← Engg.Maths-II →	→	SCD					

SCD Theory & SCD Lab - Abdul Rafi Bagalkot
 Math Sim Lab - Vijaylaxmi Sompur
 Digital Electronics Lab-I - Vijaylaxmi Sompur

Engg.Maths-II - Naganagouda.B
 Communication Skills in English - Hanamantappa Shirawar

Semester - 4

Day	9-10	10-11	11-12	12-1	1-2	2-3	3-4	4-5
Mon		DCN	DCN	uC	LUNCH BREAK			
Tue		DCN	uC	uC		← Prof.Practices Lab →		
Wed		DCN	DCN	uC		← DC&N Lab →		
Thu		DC	← PE&IC →			← uC Lab →		
Fri		DC	← PE&IC →			← TK-II →		
Sat		DC	DC	PE&IC				

DC Theory - Abdul Rafi Bagalkot

PE&IC - B M Joshi

uC Theory & Lab - Shivananda S A

DCN and DC&N Lab - Sharanappa Hiremani Prof.Practices Lab - Sharanappa Hiremani TK-II - B K Madi

Semester - 6

Day	9-10	10-11	11-12	12-1	1-2	2-3	3-4	4-5
Mon		IA	IA	Adv uP	LUNCH BREAK	← IA Lab →		
Tue		IA	Adv uP	Adv uP		← Project Work-II →		
Wed		IA	Adv uP	Adv uP				
Thu		Verilog	Embedded Systems(ES)					
Fri		Verilog	Embedded Systems(ES)				← Inplant Training →	
Sat		Verilog	Embedded Systems(ES)				← Verilog Lab →	

ES - Shashikumar B

IA theory & Lab - Farida Talikoti

Adv. uP - Vijaylaxmi Sompur

Verilog Lab - Shivananda S A

Project Work-II - Shivananda S A

Inplant Training - Shivananda S A

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 GAJENDRAGAD - 582114